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Application Note

AN2112en

Signal Over- and Undershooting

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Figure 1: e.MMC interface at 1.8 V and 200 MHz (yellow: CLK, red: DAT0) with clear reflections on DAT0. However, it is not possible to determine whether these overshoots and undershoots also occur at the input stage.

1 Abstract

Different bus systems, such as the SD and e.MMC interface, SATA or PCIe, offer various properties in terms of data transfer rates and connectivity. These systems, however, are not immune to special challenges in PCB design, despite their long-standing use. One such challenge is signal reflection, which can impact the performance and reliability of the entire system.

This note addresses signal reflections in mass storage interfaces, with particular attention to signal over- and undershooting.

2 Signal reflexions

Signal reflection occurs when a signal encounters an impedance mismatch along the transmission path. This impedance mismatch can arise from various factors, such as variations in trace impedance, connectors, and termination. When a signal encounters an impedance mismatch, a portion of the signal energy is reflected back towards the source. This reflected energy can interfere with the original signal, leading to distortions and potential signal integrity issues.

Overshoots and undershoots result from the superposition of the transmitted signal with a reflection of this signal. An overshot refers to the phenomenon where the voltage of a signal momentarily exceeds its desired amplitude before settling down to its intended level. On the other hand, an undershoot is when the voltage of a signal dips below its desired level before returning to its proper value. Both overshoots and undershoots can result in signal distortions and potentially cause erroneous data transfer or even system malfunctions. Figure 1 shows an example of overshoots and undershoots on the data line of an e.MMC.

Understanding the causes and effects of overshoots and undershoots is crucial for designing robust and reliable interfaces. Factors such as impedance mismatches, signal rise and fall times, and the characteristics of the transmission medium, all play a role in the occurrence and severity of these signal reflections. Identifying potential sources and mitigating these reflections during schematic design and PCB layout can improve overall signal integrity, reduce data errors, and improve system performance.

3 PCB design

To ensure robust signal integrity and minimize the occurrence of signal reflections, it is important to implement proper PCB design techniques. The following techniques are the most important to consider:

- Trace length matching:
  An effective technique for improving signal quality is to ensure equal trace lengths for all signals that are part of the same bus. This helps maintain consistent propagation delays and equal arrival times. While this does not prevent signal reflections, it does ensure that setup and hold times are maintained for interfaces with separate clock signals (e.g. SD and e.MMC). It also minimizes the effects of crosstalk. When tuning the trace lengths, all bus signals should still be routed in parallel as far as possible and not reach their destination via different paths.

- Impedance control and termination:
  Maintaining consistent impedance along the transmission lines is critical to minimize signal reflections. This involves careful selection of the trace width and layer stack-up. Impedance matching between the driver, receiver, and transmission line avoids the likelihood of signal reflections at the junctions.

  While the interfaces in the host and storage medium are usually already properly terminated, and the impedance of the drivers is often configurable, the main focus is on switches, buffers, and level converters, which are placed in the signal path and often have high-impedance inputs. ESD protection or an EMI filter can also cause strong reflections due to its capacitances. Therefore, diodes with low capacitance, combined with low impedance series resistors, are primarily recommended for ESD protection instead of capacitors as shown in Figure 2.

- Minimize vias:
  Vias often lead to local impedance mismatches and thus to signal reflections. The number of vias should therefore be reduced to the absolute minimum necessary, especially for high-speed signal paths. If vias are required, impedance controlled vias should be used, at least for NVMe, to ensure signal integrity. The reference plane must also be taken into account and must not be interrupted.

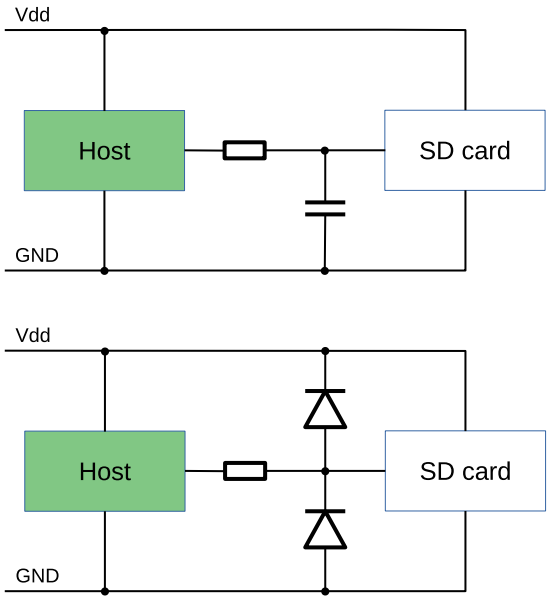

Figure 2: ESD protection for SD cards (top: capacitive load on signal line, bottom: recommended circuit). The series resistor attenuates both reflections and ESD pulses.

- Proper reference plane:
  A continuous reference plane under the signal paths is required to keep the line impedance constant, avoid electromagnetic interference, and ensure a low-impedance return path for the signals. It also reduces the probability of crosstalk.

- Avoiding stubs:
  Stubs (i.e., branches in the signal path) cause signal reflections. Stubs often occur when connecting more distant test pads or pull-up resistors and should be avoided or kept as short as possible. Test pads should be located directly next toor integrated into the trace. Pull-up resistors should be placed as close as possible to the signal lines. Because pull-up resistors have a much higher impedance than the line, the reflection caused by the resistor itself is much lower than that caused

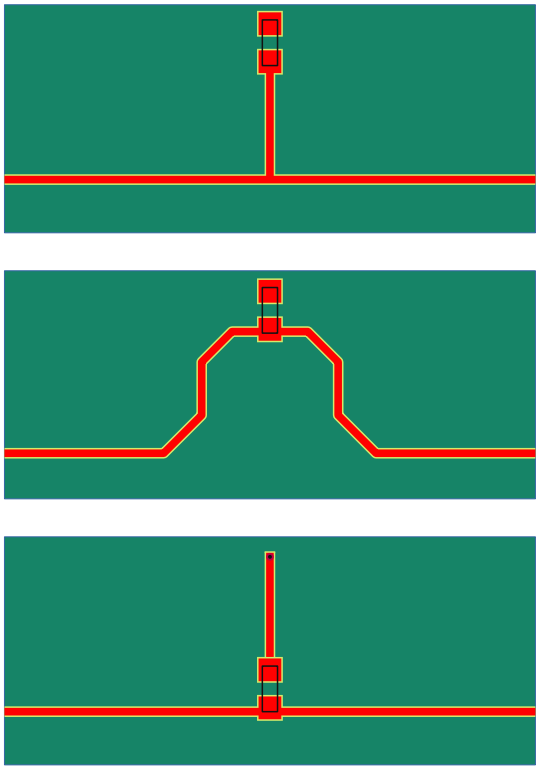

Figure 3: Three ways to connect a pull-up resistor to a signal line. Top: unfavorable design (reflections are to be expected), middle and bottom: better solutions.

by a longer stub to the resistor. Figure 3 shows different ways to connect the required pull-up resistor to the signal lines of an e.MMC or SD card.

- Avoid additional connectors:
  Each connector represents a point of impedance jump and may cause signal reflections. Minimizing the use of connectors in the signal path helps reduce the likelihood of impedance mismatch and improves overall signal integrity. If required, impedance-matched connectors should be used.

Incorporating these PCB design practices can significantly reduce signal reflections and the resulting overshoots and undershoots. Specific design considerations may vary depending on the bus system and its operating parameters. Simulation and testing of the design is recommended to ensure optimal signal integrity.

4 Dangers due to overshoot and undershoot

Swissbit often receives customer inquiries about overshoots and undershoots in SD, e.MMC and SATA. The biggest concern is that the controller of the storage medium or the host chipset is damaged due to the signal characteristics observed with an oscilloscope. Currently, Swissbit is not aware of any case where damage to the controller or host chipset has occurred.

Theoretically, there is a risk of damaging the semiconductor in the event of strong overshoot or undershoot due to *hot carrier*. However, much higher voltages than those seen with faulty matches are required to damage the semiconductor. Harmful overvoltages can be dissipated by the integrated ESD protection diodes at the signal inputs. Although the protection diodes can only dissipate a limited current without thermal or by electromigration damage to themselves, typical overshoots or undershoots do not contain the energy required to damage diodes. The specification of the maximum and minimum permissible voltages in the data sheet, therefore, refers to the normal signal level without the superimposition of the reflected component.

The dreaded latch-up effect also no longer occurs today because the input stages are hardened accordingly.

The real danger from overshoots and undershoots is the non-destructive effect. If the signal voltage exceeds the threshold voltage at which the diode begins to conduct significantly in the forward direction, the over- or undervoltage is injected directly into the device's power supply – in this case, into the controller of the storage medium. Because there are only very small electrical capacitances inside, the capacitances can only attenuate the distur-

bances, often inadequately. As a result, over- or undervoltages can lead to jitter, noise, and timing problems in adjacent output drivers. In particularly severe cases, errors occur in the CPU or RAM. Accordingly, malfunctions of the storage medium and data loss could occur.

5 Measurement

The basic issue with overshoots or undershoots is that they cannot be easily measured. Only the wave form directly at the input stage of the controller is relevant to the previously mentioned problems. However, it is not possible to measure directly at the pad of the silicon die. The first place that can typically be reached with a probe is the trace or a test pad right next to the BGA package of the controller.

From there, it is a few tenths of an inch to the solder ball, followed by a piece of trace on the substrate inside the package, a via through the substrate, a piece of bond wire, and finally where the bond wire lands on the pad of the die. Each of these transitions represents an impedance jump where a small part of the signal is reflected. Therefore, theoretically the probe would have to be placed directly on the pad to prove the existence and amplitude of a problematic overshoot or undershoot. This is 'theoretical' because placing the probe on the pad also causes an impedance change. Figure 4 shows the cross-section of a typical controller with the signal paths in a BGA package.

Thus, by measuring the signal wave form on the PCB, it is not possible to detect any overshoot or undershoot at the particular input stage. Nevertheless, such measurements are appropriate to check the amplitude and the slope and to adjust them in the transmitter, if necessary. Figure 5 shows such a control measurement at the SATA interface.

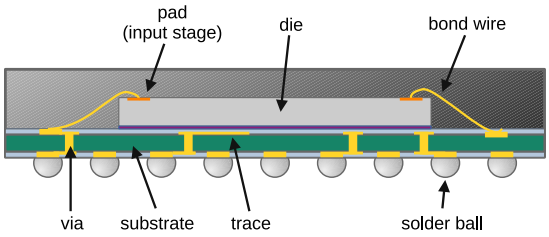

Figure 4: Cross-section of a controller in a BGA package. If the signal quality is measured close to the package, the path to the pad is still long and contains several impedance changes that can cause reflections. Therefore, no reliable statement can be made about the wave form at the pad.

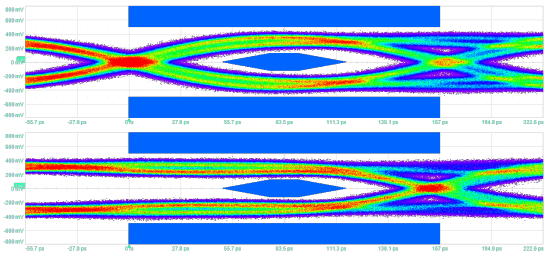

Figure 5: Eye diagram of a 6 GHz SATA-III signal measured near the receiver (top with polarity change, bottom without). Minimal reflections and no unnecessary high amplitude.

6 Summary

Overshoots or undershoots on the signal lines generally do not cause damage to the semiconductor. However, they can cause malfunctions in the circuit logic, which may well lead to data loss or other malfunctions.

Because overshoots or undershoots are difficult to detect by measurement, the golden rule for signal lines is to drive only as strongly as necessary and as weakly as possible. This can be easily checked by measuring the slope or rise time. In addition, lowering the driver strength leads to lower energy consumption and less electromagnetic interference.

If PCB design rules in section 3 are also implemented, no signal problems and disruptive influences on the safe operation of the storage medium are to be expected.

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