swissbit®

Application Note

AN2111en

SD Memory Card Design-in

[1] This work is licensed under the Creative Commons License "Attribution 4.0 International". To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/

swissbit®

Contents

1 Abstract

This guide is intended to serve as support for the integration of SD Memory Cards. Swissbit has been one of the leading suppliers of SD Memory Cards for industrial use as well as for the automotive industry for many years. This document was created from this experience. It focuses on the most common problems that may occur during the integration of an SD Memory interface.

2 Supply voltage

2.1 Voltage stabilization

During initialization and operation at Default Speed (DS), an SD memory card may require a maximum of 100 mA. When an SDXC card is configured for maximum speed (XPC bit), it is allowed to consume up to 150 mA immediately. When High Speed (HS) or Ultra High Speed (UHS-I) is enabled, consumption may increase to 200 mA or 400 mA, respectively.

Problems typically occur here during initialization. The maximum permissible current, according to the SD memory specification, refers to the average value measured over one second. When the integrated controller accesses the flash, the consumption of the controller and the flash can add up to significantly higher peak values. These peaks can be several hundred milliamps and typically last up to a millisecond. The SD memory card's power supply must be designed for these peaks and buffered with capacitors. Otherwise, the supply voltage may fall below the minimum permissible voltage. Here, the brown-out detector may be triggered and activate the write protection of the NAND flash to protect the data.

According to the SD memory specification, after the supply voltage falls below the permissible range, the power supply must be cycled, which causes the card to perform a hard reset and return to normal operation. However, because current peaks already occur during initialization, an infinite loop can occur if the supply is too weak.

2.2 Switchable supply voltage

The host should basically be able to switch the SD memory card supply voltage to force a hard reset of the SD memory card. For example, if a switch of the interface voltage (CMD11) from 3.3 V to 1.8 V fails, the return to 3.3 V may only occur after the supply voltage is switched off.

Although the SD memory specification only states 0.5 V, the voltage should drop below 0.1 V during shutdown to meet the requirements of current and future 3D NAND flashes. Therefore, the duration of the shutdown must be selected sufficiently to discharge the voltage stabilization capacitors (see section 2.1), provided that the disconnection occurs before the discharge.

2.3 Switch-on point

SD memory cards do not have high requirements for voltage ramp on power-up. The SD memory specification provides a time duration of 0.1 to 35 ms for ramp. However, it is important (as with all storage media) that the voltage rises monotonically and does not drop again before the operating voltage has been

reached. Subsequently, the minimum operating voltage of 2.7 V may only be undershot again for shutdown.

3 Signal lines

3.1 Signal quality and ESD protection

All signal lines between the chipset and the SD memory slot should have exactly the same length and be routed via a ground plane to ensure identical impedances and sufficient noise immunity, especially for the SDR104 mode. The number of vias in a signal line should not exceed two. For larger distances between chipset and SD memory slots, a series resistor should be provided at least in the clock path to attenuate reflections and should have a value of 0 – 22 Ω.

The insertion of additional capacitances in the signal lines should be avoided, as these increase the temperature dependence of the signal propagation. For ESD protection, fast diodes in combination with series resistors in the signal path and a suppressor diode are more suitable than low passes, consisting of resistors and capacitors, as shown in figure 1.

If capacitors are, however, inserted into the signal path, their values should not exceed 4.7 pF. In addition, the same capacitance must then be applied to all signals (CLK, CMD, and DAT[3:0]). Sometimes a capacitor is only connected to CLK to improve the EMC properties, which then leads to a delay of the signal compared to CMD and DAT[3:0], and can result in read errors, which occur frequently after temperature changes if no renewed tuning (CMD19) is carried out.

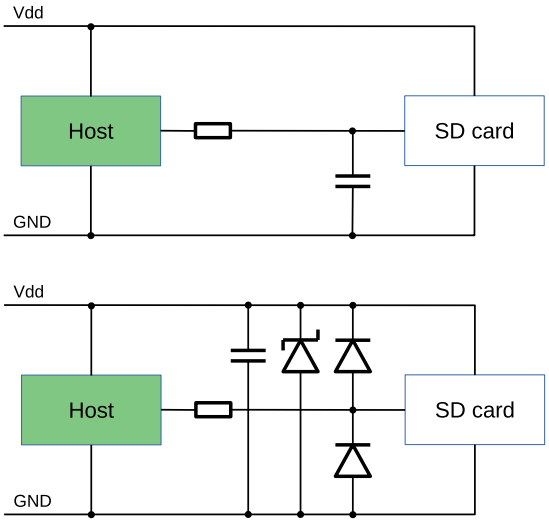

Figure 1: ESD protection (top: capacitive load on signal line, bottom: recommended circuit)

3.2 Level converter

When using bidirectional level converters between the host chipset and the SD memory card, the state after switching on the supply voltage must be checked in order not to activate the SPI mode of the SD memory card unintentionally. This happens when a low level is applied to DAT3 while CMD0 is being sent.

Typically, both sides of a level converter have pull-up resistors that should prevent this. However, it may happen that the supply voltage is applied to the level converter earlier than to the pull-up resistors. In this case, the bidirectional level converter would detect and drive a low level in both directions.

A level change is performed by a typical converter at an externally applied drive strength of a few milliamperes, but this cannot be applied by the pull-up resistors. Thus, DAT3 remains at low level, and the board switches to SPI mode with CMD0 and no longer responds to commands.

Again, this problem may not become apparent immediately, because many SD memory cards drive (unintentionally) the outputs high for a brief moment on power-up during the supply voltage rise, which causes the level converter to switch. Thus, the problem may not be noticed until the SD memory card type is changed, or isolated failures occur in the field. A possible remedy is to provide the enable line of the level converter with a low-pass filter. This allows the converter to start after the high level is applied on both sides by the pull-up resistors. Alternatively, the host can briefly

drive a high level to DAT3 before transmitting CMD0. However, this is usually only possible on systems that do not boot from the SD memory card.

3.3 Floating Clock

According to the SD memory specification, all signals except the clock, must be provided with pull-up resistors to prevent floating. Since the clock signal is only driven from the host side, unlike the other signales, it does not reuqire a pull-up resistor. However, this assumes that the signal is driven by the host at all times. If the clock floats, electromagnetic interference can cause the card's PLL to generate an internal clock that is above the maximum permissible frequency, which can cause the SD memory card to malfunction or hang up.

A floating of the clock occurs if the host does not initialize the SD memory interface immediately when the supply voltage is switched on. Another source of error is the transfer of program execution between the different stages of the boot loader. Some systems switch the clock output to a high impedance state here. The Raspberry Pi family, for example, is a well-known representative of this group.

It is therefore recommended to check the expected behavior of the host with an oscilloscope and, if necessary, to ensure a defined state of the clock signal with a 100 kΩ pull-down resistor or to provide such a placement option.

3.4 Pull-up resistors

The pull-up resistors for CMD and DAT must be between 10 kΩ and 100 kΩ. It has been shown that internal pull-up resistors of the chipsets can have too large values, or they can be switched off briefly when the interface configuration is changed, which can lead to communication errors. Therefore, only external pull-up resistors should be used.

If the power supply of the SD memory card is switchable, as recommended in the 2.2 section, the power supply for the pull-up resistors must be connected behind the switch. Otherwise, resetting of the card can be prevented by the current continuing to feed the board through the pull-up resistors and the internal ESD diodes as shown in Figure 2.

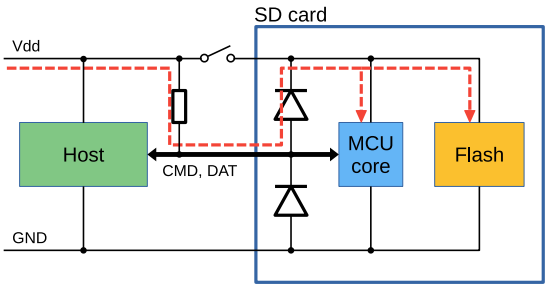

Figure 2: Card powered via pull-up resistors and ESD diodes

4 Protocol issues

4.1 CMD11 – Voltage Switch

To increase the interface speed to UHS-I, it is necessary to change the signal level from 3.3 V to 1.8 V in advance. This is done with the command *CMD11*. The SD memory specification must be followed exactly; otherwise, the synchronization of the SD memory card with the new 1.8 V clock of the host may fail, whereupon the card hangs or shows other malfunctions.

Figure 3 shows the correct procedure: After the host issues the CMD11 command and the card acknowledges receipt with R1, the card drives the CMD line and DAT lines low. Then the host stops the 3.3 V clock for at least 5 milliseconds. After that, the host restarts the clock, but now with a level of 1.8 V. Within one millisecond the card confirms the successful switching by driving the DAT lines with high level. Only now the host may stop the clock again.

During the switching sequence, it is absolutely necessary that there is no activity on the clock line in the *A* section. Even a short voltage spike, possibly generated by the host when switching the voltage, may cause the card to misbehave.

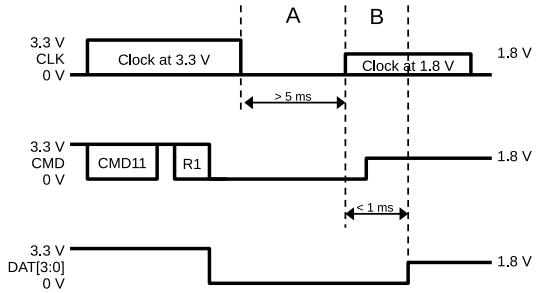

Figure 3: CMD11 voltage switch sequence

In the *B* section, the clock must run continuously without missing even one clock cycle.

Some hosts that violate the specification in the *A* or *B* sections also exhibit different behavior at each CMD11, resulting in an SD memory card malfunction occurring so infrequently that there is a risk of only becoming aware of errors in the field. The figure 4 shows such a case.

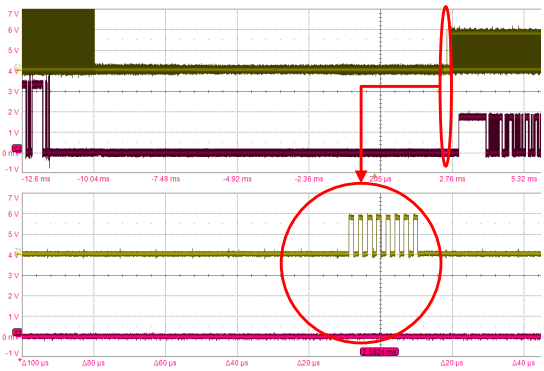

Figure 4: Protocol violation during CMD11 (green shades: CLK, red shades: CMD)

Before the clock runs continuously on 1.8 V, the host sends several clock cycles, which vary in number and position each time. Because of this widespread problem with CMD11, it is recommended to check the switching in the finished circuit with an oscilloscope.

5 Qualification

Since the SD memory interface does not have a return clock, like an eMMC, CMD19 provides the option of requesting a test pattern from the SD memory card for higher transfer rates in order to determine the optimum sampling time for the host in the read direction. For transfer modes such as SDR50, DDR50 and SDR104, the entire expected temperature range should be checked in the field, even if communication with the SD memory card remains error-free when initialization or tuning (CMD19) took place at the other end of the temperature range.

CONTACT US

Headquarters	**Swissbit AG** Industriestrasse 4 9552 Bronschhofen Switzerland	Tel. +41 71 913 03 03 sales@swissbit.com
Germany (Berlin)	**Swissbit Germany AG** Bitterfelder Strasse 22 12681 Berlin Germany	Tel. +49 30 936 954 0 sales@swissbit.com
Germany (Munich)	**Swissbit Germany AG** Leuchtenbergring 3 81677 Munich Germany	Tel. +49 30 936 954 400 sales@swissbit.com
North and South America	**Swissbit NA Inc.** 238 Littleton Road, Suite 202B Westford, MA 01886 USA	Tel. +1 978-490-3252 salesna@swissbit.com
Japan	**Swissbit Japan Co., Ltd.** CONCIERIA Tower West 2F 6-20-7 Nishishinjuku Shinjuku City, Tokyo 160-0023 Japan	Tel. +81 3 6258 0521 sales-japan@swissbit.com
Taiwan	**Swissbit Taiwan** 3F., No. 501, Sec.2, Tiding Blvd. Neihu District, Taipei City 114 Taiwan, R.O.C.	Tel. +886 912 059 197 salesasia@swissbit.com
China	**Swissbit China**	Tel. +886 958 922 333 salesasia@swissbit.com

Disclaimer:
The information in this document is subject to change without notice. Swissbit AG ("SWISSBIT") assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SWISSBIT makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SWISSBIT does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SWISSBIT products in applications not intended by SWISSBIT, said customer must contact an authorized SWISSBIT representative to determine SWISSBIT willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SWISSBIT.

ALL PRODUCTS SOLD BY SWISSBIT ARE COVERED BY THE PROVISIONS APPEARING IN SWISSBIT'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SWISSBIT MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT, AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.