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Application Note

AN2107en

NAND flash endurance testing

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Contents

1 Abstract

Typical application scenarios for NAND flash memory assume a service life of 3–5 years and in some cases even significantly longer. The flash type to be used (SLC, pSLC, MLC, TLC, QLC) is selected accordingly, which has the necessary endurance, i. e. the lifespan measured in erase and programming cycles.

Here, the "Lifetime Monitoring Tool" supports, which can be downloaded from the Swissbit FTP server [1], to use the target application to measure the wearout or the required TBW[2] over the lifespan.

If the specified endurance is to be checked as part of the qualification of a NAND flash memory for a project, the rate of aging has a significant influence on the result. The effects of aging too quickly and how they can be avoided are shown below.

2 The Floating Gate

The figure 1 shows schematically the cross section of a NAND flash cell. This cell corresponds to the construction of a field effect transistor, where a further conductive layer was installed between the control gate and the substrate. This layer is surrounded on all sides by dielectrics (SiO_2, ONO). Since it has no electrically conductive connection, the layer is called "floating gate".

[2] "Terabytes written" – the minimum amount of data that can be written to an SSD in a standardized test

If the floating gate carries no charge, the NAND flash cell behaves like a field effect transistor: Applying a positive voltage to the control gate creates an electrostatic field between the substrate and the control gate. Accordingly, free electrons concentrate on the top of the substrate and form a channel between "source" and "drain". The transistor conducts.

However, if the floating gate carries a negative charge by free electrons, the electrical field that is generated by the positive voltage at the control gate is compensated, and an electrical field no longer acts on the free charge carriers in the substrate. As a result, no channel forms and the transistor does not conduct.

In this example, the floating gate has two states: Charged and uncharged (neutral). This enables the cell to store a single bit. With MLC memory, two bits can be stored per cell. Accordingly, the floating gate can carry four different amounts of charge. Various voltages are applied to the control gate to read out the information.

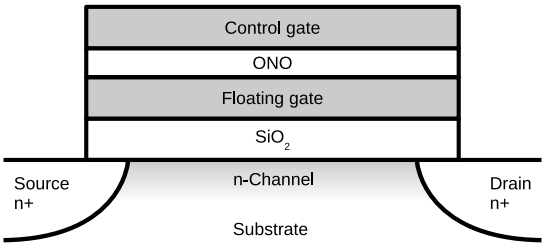

Figure 1: NAND flash cell

3 Fowler-Nordheim Tunneling

In order to program the cell, i. e. to place electrons into the floating gate, the silicon oxide insulation layer must be overcome. The "Fowler-Nordheim tunneling" is used here: By applying a strong electrostatic field between the substrate and the control gate, electrons can tunnel through the potential barrier of the insulation material. This is a quantum mechanical effect that enables the electrons to overcome or tunnel through a potential barrier that is higher than the energy of the electrons.

The same procedure is used to delete the information in the cell, i. e. to remove the electrons, but with the opposite polarity. Since a positive voltage is applied to the substrate, all cells in the environment are affected. This is the reason why only entire flash blocks can be deleted together, while the programming can be done in a more granular way.

Figure 2 shows the programming process using the Fowler-Nordheim tunneling and figure 3 the corresponding erasing process. If more than one bit is stored per cell (with MLC, TLC, QLC), more than two different potentials must be achieved. To do this, the electric field is applied several times with short pulses. After each pulse, the potential reached is read out. When the required number of electrons in the floating gate is reached, the programming process stops.

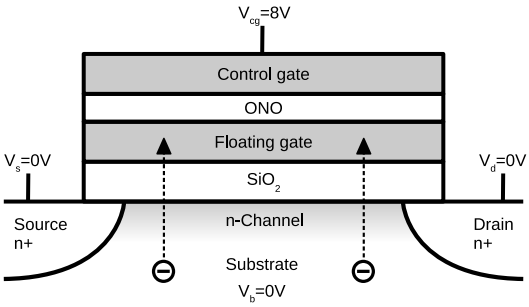

Figure 2: Programming

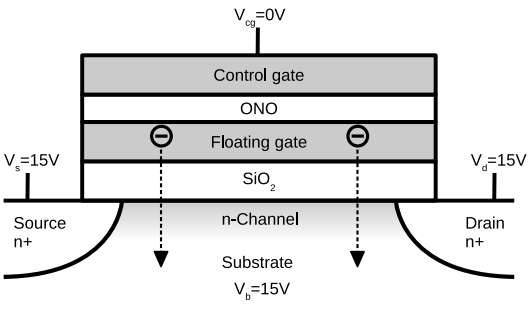

Figure 3: Erasing

4 Cell Degradation

The tunnel oxide is permanently damaged by the program and erase operations. Atomic bonds in the oxide and at the interface of the substrate are broken during this stress, so-called "defects". This creates energy states that can be occupied by electrons or holes (so-called "traps"). These defects weaken the potential barrier. The probability that an electron can escape from the floating gate in a certain time increases. This effect is called "trap assisted tunneling" (TAT) and is the root cause of the "stress induced leakage current" (SILC). The associated loss of charge in the floating gate is the reason for the exponential decrease in the "data retention time" over the number of program and erase cycles. The data retention time describes the period of time over which the flash can hold the stored information without the information having to be refreshed by copying. Typically, the endurance is specified that the flash can hold the data for at least 10 years up to a wearout of 10 % of the permissible program and erase cycles and 1 year at the maximum number of cycles.

The defects in silicon oxide are not only occupied by electrons from the floating gate that flow away unintentionally, but also by the electrons that tunnel through the oxide during program and erase operations. The number of electrons that bound to a defect shows a square root dependence on the number of program and erase cycles, while the detrapping from a defect occurs with a logarithmic dependence (ln) of time and accelerates strongly at elevated temperature [2].

Figure 4 shows charge carriers which, due to the large number of program and erase cycles, are trapped at defects in a short time. On the one hand, this accumulation of predominantly negative charges increases the threshold voltage that must be applied to the control gate in order to create a conductive channel. As a result, the states of the floating gates can no longer be clearly determined. This particularly affects the erased state. On the other hand, the detrapping leads to a reduction in the threshold voltage, which also means that

the states can no longer be identified and the stored data is lost. In addition, the more negative charges are trapped in the oxide, the greater the stress for the tunnel oxide when the cell is erased.

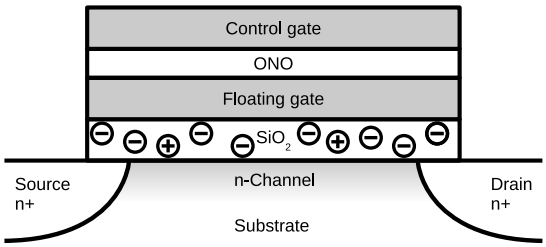

Figure 4: Trapped charges in tunnel oxid

5 Stress Tests

If the specified durability is to be checked as part of the qualification of a NAND flash memory, it must be ensured that the memory does not prematurely fail due to the accumulation of electrons in the tunnel oxide. According to JEDEC JESD22-A117 [3], durability tests must be performed with care to avoid the unrealistic stress that would occur if the test reached the specified storage life in only a few days.

The flash must therefore have enough time to recover during stress tests. This can be done either by regular breaks, a lower writing speed or an increased flash temperature. While flash memory is relatively insensitive to a quick sequence of program and erase cycles at the beginning of its lifetime, the sensitivity increases significantly with increasing defects in the tunnel oxide [4].

If rapid testing is required, it is possible with all current flash technologies to age the memory at +85 °C within 1000 hours to the specified number of cycles. It is only necessary to ensure that all flash blocks age at approximately the same speed, which is best done by sequential writing across the entire address space. If the host cannot be operated at this temperature, or if the storage medium cannot be operated remotely in an oven, it is also sufficient to just heat the flash components – e. g. with heating tongs. Please note that the data retention time at the end of the service life at +85 °C is only a few days. As soon as the writing test has ended, the temperature should be reduced.

6 Summary

The damage to the memory cells of flash memories depends on the number of program and erase cycles that have taken place and on the speed at which these cycles take place. With the typical lifetime of a flash memory medium, the cycles are mostly evenly distributed over a period of at least three years. The period between two cycles is then sufficient for the charges in the tunnel oxide to detrap, and the flash reaches its specified number of cycles. In the case of an atypically short cycle time (especially in the case of qualification tests), there must be sufficient time between the cycles for the cells to recover and / or the temperature must be increased in order to achieve the specified service life.

Swissbit AG will be happy to assist you in choosing suitable test methods.

References

[1] **ftp://public:public@ftp.swissbit.com/SFxx_LTM_Tool/**

[2] Mielke, N.; Belgal, H.; Kalastirsky, I. et al. *Flash EEPROM threshold instabilities due to charge trapping during program/erase cycling*; IEEE Transactions on Device and Materials Reliability, vol. 4, no. 3, pp. 335–343, 2004.

[3] JEDEC Standard JESD22-A117C. *Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test*; Technical Report; JEDEC Solid State Technology Association: Arlington, VA, USA, 2011.

[4] Spinelli, A.; Compagnoni, C.; Lacaita, A. Reliability of NAND Flash Memories: Planar Cells and Emerging Issues

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