swissbit®

Product Data Sheet

Industrial M.2 PCIe SSD

N3002 M.2 Series

PCIe 4.0, 3D TLC

Industrial Temperature Grade

Date: May 13, 2024
Revision: 1.00

powersafe™

Made in Germany

Contents

N3002 M.2 Series – Industrial M.2 PCIe SSD 240 GBytes up to 2 TBytes

1. Product Summary

- **Capacities:** 240 GBytes, 480 GBytes, 960 GBytes, 1920 GBytes
- **Form Factor:** PCI Express M.2 2280 (80 mm x 22 mm x 3.8 mm)
- **Compliance[1]:** PCI Express (PCIe) Base Specification Revision 4.0
- **Interface:** Gen4 x 4 Lanes
  - Drive operates in x1 mode in x1 M.2 PCIe slots
  - Drive operates in x2 mode in x2 M.2 PCIe slots
  - Drive operates in x4 mode in x4 M.2 PCIe slots
- **Command Sets:** Supports NVMe 1.4
- **Target Performance:**
  - Read Performance: Sequential Read up to 3,850 MBytes/s, Random Read 4K up to 455,3900 IOPS
  - Write Performance: Sequential Write up to 3,340 MBytes/s, Random Write 4K up to 457,000 IOPS
- **Operating Temperature Range[2]:**
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:**
  - Industrial: -40 °C to 85 °C
- **Power:**
  - Power States PS0, PS1, PS2, PS3 and PS4
  - Thermal Throttling supported
- **Data Retention[3]:** 10 Years @ Life Begin; 1 Year @ Life End, @40°C
- **Shock/Vibration:** 1,500 g / 50 g
- **High-Performance Processor with Integrated, Parallel Flash Interface Engines:**
  - Triple-Level Cell (TLC) 3D NAND Flash
  - DDR4 DRAM based Controller architecture
  - 240 bit LDPC correction per 2 kByte
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 3,000,000 hours
  - Data Reliability: < 1 non-recoverable error per 10^{16} bits read

[1] To check the compatibility of the customer system and the storage device is part of the customer's responsibility. Swissbit can provide guidance and support on request.
[2] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 110°C (industrial temperature drive).
[3] NAND Flash suppliers refer to JEDEC JESD47 and JESD22 for Data Retention testing. Based on the information provided by the NAND Flash suppliers, Data Retention is targeted as shown

2. Product Features

- Diagnostic features
- Life end read only mode
- RAID engine
- Drive self-test
- Data Care Management
  - Active: Adaptive Read Refresh
  - Passive: Background Media Scan
- Active State Power Management (ASPM) Support
- In-Field Firmware Update[4]
- Adaptive Thermal control
- DRAM-Buffer
- Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T., Telemetry)
- SMBus[5] (NVMe Management Interface Basic Management Command, NVMe-MI v1.2)
- 30 µinch (0.8 µm) Gold-Plated Connector (IPC-6012C Class 2 Compliant)
- End-to-End (E2E) Data Protection
- powersafe™ Functionality (Power Loss Protection Level 3)
- Controlled "Locked" BOM
- RoHS / REACH Compliant
- Swissbit Device Manager Tool (SBDM)

3. Security features

- AES256 encryption
- TCG OPAL 2.0
- Secure Boot
- Crypto erase
- IEEE 1667

[4] The support of In-Field FW update capabilities on host systems is recommended.
[5] SMBus commands are only processed in operational power states.

4. Ordering Information

Table 1: Standard Product List

Capacity	Part Number	Numbers of Lanes
240 GBytes	SN3002Mx240GI-yMA4-zGA-STD	4
480 GBytes	SN3002Mx480GI-yMA2-zGA-STD	
960 GBytes	SN3002Mx960GI-yMA4-zGA-STD	
1920 GBytes	SN3002Mx1T92I-yMA4-zGA-STD	

x = Form Factor; y = Product Generation; z= Firmware Revision

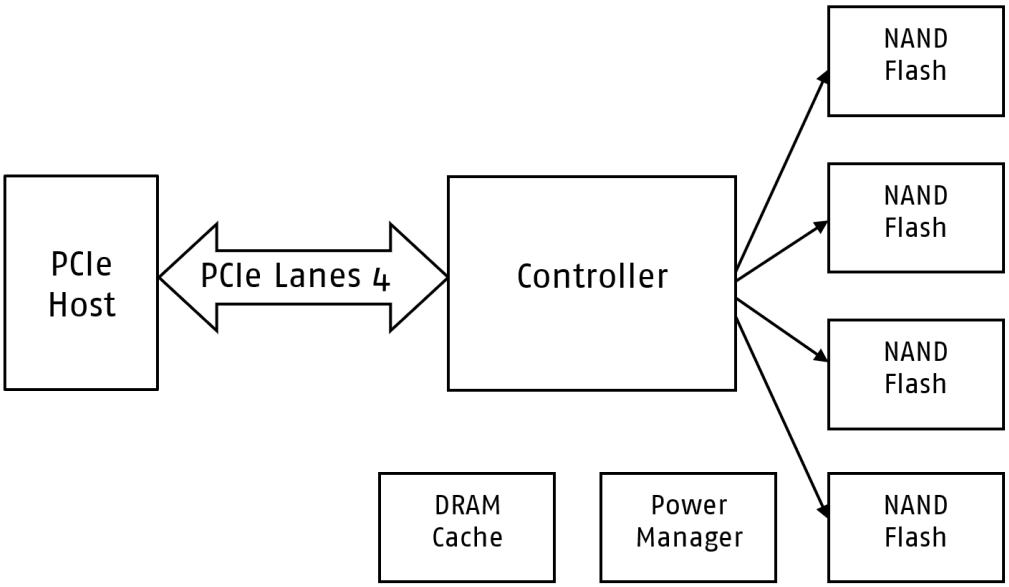
Table 2: Available Part Numbers

Capacity	Industrial Temperature
	2280 with PowerSafe
240 GBytes	SN3002MD240GI-1MA4-1GA-STD
480 GBytes	SN3002MD480GI-1MA2-1GA-STD
960 GBytes	SN3002MD960GI-1MA4-1GA-STD
1920 GBytes	SN3002MD1T92I-1MA4-1GA-STD

5. Product Description

The Swissbit® N3002 M.2 Solid State Drive (SSD) leverages the M.2 standard and NVMe standard to support a PCIe electrical interface as well as AES encryption, E2E data protection and TCG Opal standards. The NVMe controller and the newest 3D NAND flash technology provides robust, non-volatile storage solution for today's embedded computing applications. A functional block diagram of the N3002 M.2 SSD is provided below in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Figure 1: N3002 M.2 Functional Block Diagram



The N3002 M.2 SSD incorporates a 75-position edge connector with M key to support host read/write, control, and power activity per the applicable JEDEC specification.

The on-board NVMe controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support PCIe interface speeds and utilizes a dual processing core, providing an optimum balance between read/write performance, Data Care Management, and power fail protection.

Swissbit's N3002 M.2 SSDs deliver an impressive IOPS rate and highest endurance by combining 3D NAND flash technology with a high-end controller architecture, firmware, and an optimized configuration. The SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance). This performance is achieved through a 4-channel flash controller and 4-lane PCIe interface.

An on-controller LDPC Error Correction Code (ECC) engine provides the N3002 M.2 hardware ECC, which is capable of correcting up to 240 bits per 2 KByte page. This engine, combined with Swissbit's Data Care Management firmware, provides both passive and active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, and Dynamic Block Remapping.

The Swissbit N-30m2 P offers additional powersafe™ functionality. These drives contain an array of holdup capacitors designed to supply voltage to the controller long enough for data hardening to complete. If the voltage drops below a specified threshold, the PFAIL signal is asserted, notifying the controller of the voltage loss. The controller then begins the process of hardening data and switches the power supply to the power manager from the host to the capacitor array. This allows the controller to complete any writes that were in progress at the time of power loss.

Related Documentation

- NVM Express – Revision 1.4, (https://nvmexpress.org/)
- PCI Express M.2 standard – PCI Express M.2 Specification, Revision 3.0, June 26, 2019 (https://pcisig.com)

5.1 Performance Specifications

The N3002 M.2 read/write sequential and random CDM performance benchmarks are detailed in Table 3.

Table 3: Read/Write Performance[6]

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
240 GBytes	3,650	1,480	108,300	177,500
480 GBytes	3,790	2,820	210,000	298,800
960 GBytes	3,850	3,340	392,800	457,000
1920 GBytes	3,790	3,330	455,900	394,300

5.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in Table 4.

Table 4: Current Consumption[7]

Capacity	Sequential Read	Sequential Write	Random Read 4k	Random Write 4k	Idle[8]	PS3[8]	PS4[8]	Unit
240 GBytes	1,120	920	730	910	50	12	2	mA
480 GBytes	1,140	1,210	860	1,130				
960 GBytes	1,170	1,450	1,080	1,270				
1920 GBytes	1,160	1,610	1,150	1,340				

[6] The values are measured using Crystal Disk Mark 8 with a file size of 1GiB. Performance depends on flash type and number, file/cluster size, and burst speed.
[7] All values are typical total values recorded at 25 °C and 3.3V power supply
[8] Measured with enabled ASPM L1.2

5.3 Environmental Specifications

5.3.1 Recommended Operating Conditions

The recommended operating conditions for the N3002 M.2 SSD are provided in Table 5.

Table 5: Recommended Operating Conditions[9]

Parameter	Value
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V ± 5%

5.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in Table 6.

Table 6: Recommended Storage Conditions

Parameter	Value
Industrial Storage Temperature	-40 °C to 85 °C

5.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in Table 7.

Table 7: Shock, Vibration and Humidity

Parameter	Value
Non-Operating Shock	1,500 *g*, 0.5 ms pulse duration, half-sine wave (IEC 60068-2-27 and JESD22-B110 cond. B)
Non-Operating Vibration	50 *g*, 80-2,000 Hz, 3 axes, 12 cycles (IEC 60068-2-6, MIL-STD-883 H Method 2007.3)
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B)

[9] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 110°C (industrial temperature drive).

5.4 Regulatory Compliance

The N3002 M.2 devices comply with the regulations / standards listed in Table 8.

Table 8: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE – 2014/30/EU FCC – 47 CFR Part 15 UKCA – S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

5.5 Mechanical Specifications

Physical dimensions are detailed in Table 9. Figure 3 on page 13 illustrates the N3002 M.2 dimensions.

Table 9: Physical Dimensions

Physical Dimensions		Unit
Length	80.00±0.15	mm
Width	22.00±0.15	
Thickness (nominal)	3.8	
Weight (Max Capacity)	≤ 9.0	g

5.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 10: Reliability

Parameter	Value
MTBF (at 25 °C)	> 3,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10^{16} Bits Read
Data Retention	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) for different application scenarios is provided in Table 11.

Table 11: Endurance[10, 11]

Capacity	Sequential		Client		Enterprise	
	TBW	DWPD[12]	TBW	DWPD[12]	TBW	DWPD[12]
240 GBytes	856	3.26	271	1.03	207	0.79
480 GBytes	1,684	3.20	503	0.96	379	0.72
960 GBytes	3,334	3.17	903	0.86	699	0.66
1920 GBytes	6,774	3.22	1,399	0.67	1,620	0.77

5.7 Drive Geometry Specification

The N3002 M.2 drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown in Table 12.

Table 12: Drive Geometry

Raw Capacity	User Capacity[13]	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
256 GBytes	240 GBytes	468,862,128	240,057,409,536
512 GBytes	480 GBytes	937,703,088	480,103,981,056
1024 GBytes	960 GBytes	1,875,385,008	960,197,124,096
2048 GBytes	1920 GBytes	3,750,748,848	1,920,383,410,176

[10] Client and Enterprise workloads follow the JEDEC JESD219 standard. Enterprise workload values are measured based on 240 hours of runtime. 1 TByte = 10^{12} bytes

[11] According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.

[12] DWPD values are based on a service life of 3 years

[13] 1 GByte = 10^9 bytes

6. Electrical Interface

This 75-position m.2 connector (Figure 2) incorporates M key for Socket 3 PCIe-based SSDs and follows the applicable PCIe m.2 specification. The signal/pin assignments and descriptions are listed in the following Table 13.

Figure 2: N3002 M.2 Electrical Interface

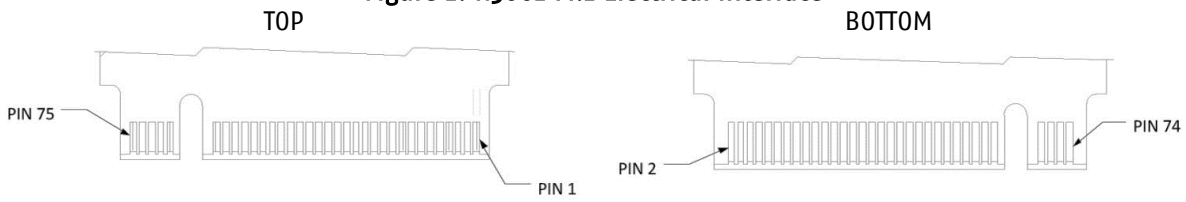


Table 13: Pin Assignment, Name and Description

Description	Assignment	Pin	Pin	Assignment	Description
Config_3	GND	1	2	+3.3V	3.3V Source
Ground	GND	3	4	+3.3V	3.3V Source
PCIe TX Differential Signal	PETn3*	5	6	NC	No Connect
PCIe TX Differential Signal	PETp3*	7	8	NC	No Connect
Ground	GND	9	10	DAS/DSS	DEVACT Device Activity Signal
PCIe RX Differential Signal	PERn3*	11	12	+3.3V	3.3V Source
PCIe RX Differential Signal	PERp3*	13	14	+3.3V	3.3V Source
Ground	GND	15	16	+3.3V	3.3V Source
PCIe TX Differential Signal	PETn2*	17	18	+3.3V	3.3V Source
PCIe TX Differential Signal	PETp2*	19	20	NC	No Connect
Config_0	GND	21	22	NC	No Connect
PCIe RX Differential Signal	PERn2*	23	24	NC	No Connect
PCIe RX Differential Signal	PERp2*	25	26	NC	No Connect
Ground	GND	27	28	NC	No Connect
PCIe TX Differential Signal	PETn1*	29	30	NC	No Connect
PCIe TX Differential Signal	PETp1*	31	32	NC	No Connect
Ground	GND	33	34	NC	No Connect
PCIe RX Differential Signal	PERn1*	35	36	NC	No Connect
PCIe RX Differential Signal	PERp1*	37	38	NC	No Connect
Ground	GND	39	40	SMB_CLK	SMBus Clock
PCIe TX Differential Signal	PETn0*	41	42	SMB_DATA	SMBus Data
PCIe TX Differential Signal	PETp0*	43	44	ALERT#	SMBus Alert Notification
Ground	GND	45	46	NC	No Connect
PCIe RX Differential Signal	PERn0*	47	48	NC	No Connect
PCIe RX Differential Signal	PERp0*	49	50	PERST#	PE-Reset (Functional Reset)
Ground	GND	51	52	CLKREQ#	Clock Request Signal; L1 PM
PCIe Reference Clock Signal	REFCLKn	53	54	NC	PCIe PME Wake
PCIe Reference Clock Signal	REFCLKp	55	56	NC	MFG Data

Ground	GND	57	58	NC	MFG Clock
Mechanical Notch M	-	59-65	60-66	-	Mechanical Notch M
No Connect	NC	67			
Config_1	NC	69	68	NC	32.768 kHz Clock Supply
Ground	GND	71	70	3.3V	Supply Pin, 3.3V
Ground	GND	73	72	3.3V	Supply Pin, 3.3V
Config_2	GND	75	74	3.3V	Supply Pin, 3.3V

*TX (transmit) and RX (receive) pins are labeled from the SSD view and must be connected with the reversed RX and TX signals of the host (i.e., TX to RX and RX to TX).

7. Package Mechanical

Figure 3: N3002 M.2 2280 dimensions in mm

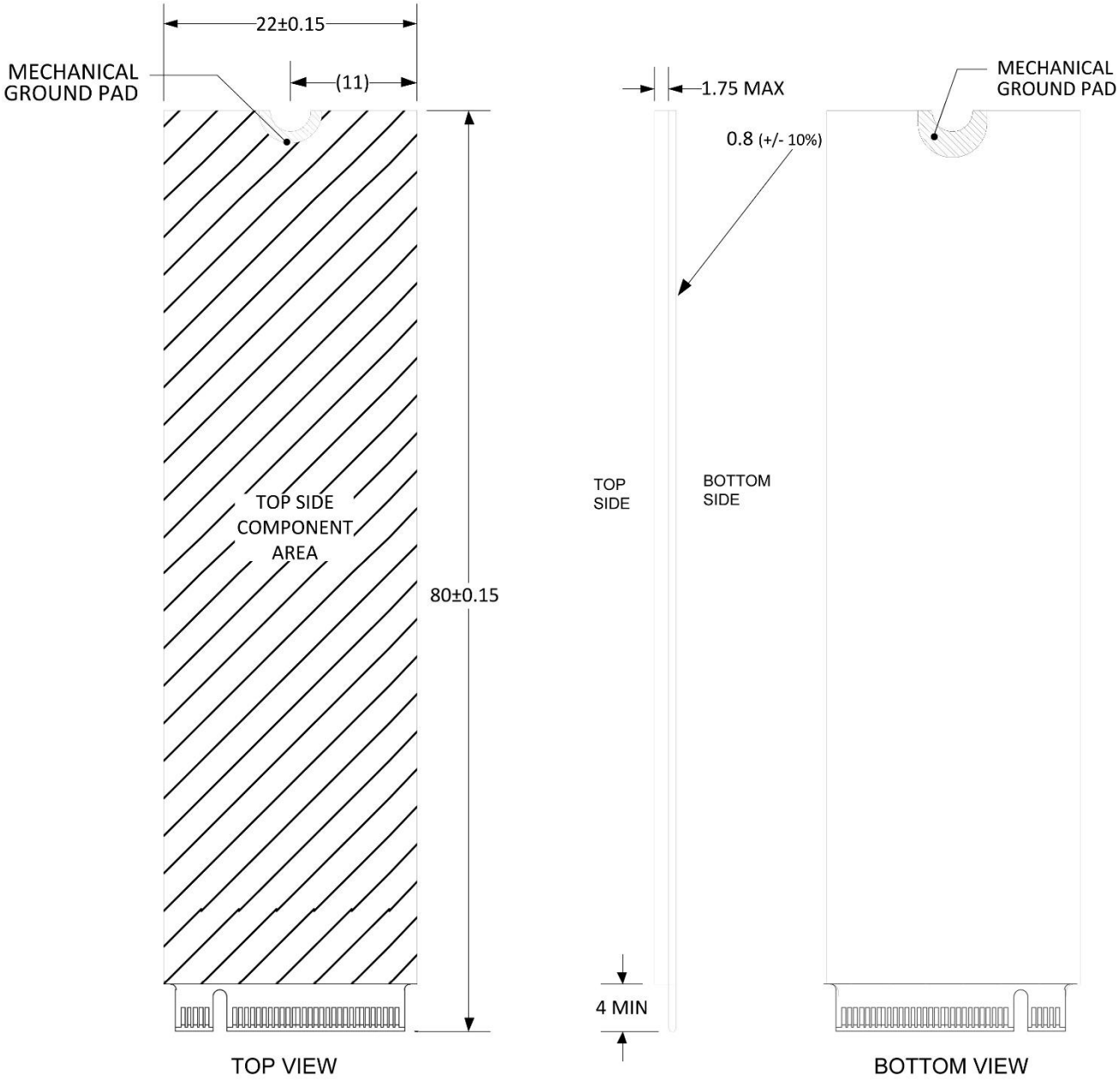
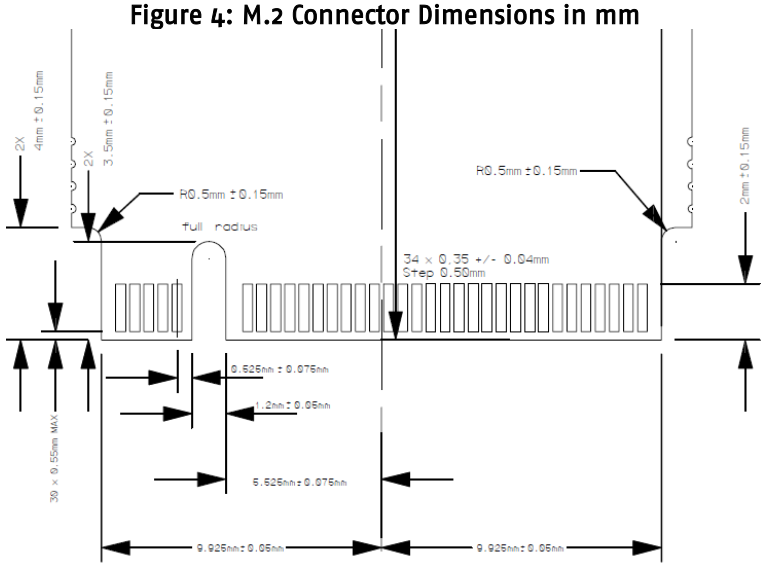


Figure 4: M.2 Connector Dimensions in mm



8. NVMe Commands

This section provides information on the NVMe commands supported by the SSD. The commands are issued by loading the DWords in the command block with the supplied parameter, and then writing the command code to the register. See the following Table 14 for a list of NVMe commands the device supports. For details about setting up the command registers, see the latest NVMe Specification.

Table 14: NVMe Command Set – Supported Commands

Command	Code
Admin Command Set	
Delete I/O Submission Queue	00h
Create I/O Submission Queue	01h
Get Log Page	02h
Delete I/O Completion Queue	04h
Create I/O Completion Queue	05h
Identify	06h
Abort	08h
Set Features	09h
Get Features	0Ah
Asynchronous Event Request	0Ch
Firmware Commit	10h
Firmware Image Download	11h
Device Self-test	14h
Format NVM	80h
Sanitize	84h
NVM Command Set	
Flush	00h
Write	01h
Read	02h
Write Uncorrectable	04h
Compare	05h

Command	Code
Write Zeroes	08h
Dataset Management	09h

Table 15: NVMe Set/Get Features – Supported Features

Feature	FID
Arbitration	01h
Power Management	02h
LBA Range Type	03h
Temperature Threshold	04h
Error Recovery	05h
Volatile Write Cache	06h
Number of Queues	07h
Interrupt Coalescing	08h
Interrupt Vector Configuration	09h
Write Atomicity Normal	0Ah
Asynchronous Event Configuration	0Bh
Autonomous Power State Transition	0Ch
Timestamp	0Eh
Host Controlled Thermal Management	10h
Non-Operational Power State Config	11h
Software Progress Marker	80h

Table 16: Supported Log Pages

Log Page	Log Identifier
Error Information	01h
SMART/Health Information	02h
Firmware Slot Information	03h
Commands Supported and Effects	05h
Device Self-Test Log	06h
Telemetry Host-Initiated	07h
Telemetry Controller-Initiated	08h
Endurance Group Information	09h

9. Identify Device Information

The following table describes the 4096 bytes of data the drive returns for the Identify command (06h).

Table 17: Identify Namespace Data Structure (CNS 00h)

Byte(s)	Default Value	Data Field Type Information
0-7	XXXXh[14]	Namespace Size (NSZE)
8-15	XXXXh[14]	Namespace Capacity (NCAP)
16-23	XXXXh[14]	Namespace Utilization (NUSE)
24	00h	Namespace Features (NSFEAT)
25	00h	Number of LBA Formats (NLBAF)
26	00h	Formatted LBA Size (FLBAS)
27	00h	Metadata Capabilities (MC)
28	00h	End-to -end Data Protection Capabilities (DPC)
29	00h	End-to -end Data Protection Type Settings (DPS)
30	00h	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	00h	Reservation Capabilities (RESCAP)
32	80h	Format Progress Indicator (FPI)
33	01h	Deallocate Logical Block Features (DLFEAT)
34-35	0000h	Namespace Atomic Write Unit Normal (NAWUN)
36-37	0000h	Namespace Atomic Write Unit Power Fail (NAWUPF)
38-39	0000h	Namespace Atomic Compare & Write Unit (NACWU)
40-41	0000h	Namespace Atomic Boundary Size Normal (NABSN)
42-43	0000h	Namespace Atomic Boundary Offset (NABO)
44-45	0000h	Namespace Atomic Boundary Size Power Fail (NABSPF)
46-47	0000h	Namespace Optimal IO Boundary (NOIOB)
48-63	All 00h	NVM Capacity (NVMCAP)
64-65	0000h	Namespace Preferred Write Granularity (NPWG)
66-67	0000h	Namespace Preferred Write Alignment (NPWA)
68-69	0000h	Namespace Preferred Deallocate Granularity (NPDG)
70-71	0000h	Namespace Preferred Deallocate Alignment (NPDA)
72-73	0000h	Namespace Optimal Write Size (NOWS)
74-91	All 00h	Reserved
92-95	00000000h	ANA Group Identifier (ANAGRPID)
96-98	000000h	Reserved
99	00h	Namespace Attributes (NSATTR)
100-101	0000h	NVM Set Identifier (NVMSETID)
102-103	0000h	Endurance Group Identifier (ENDGID)
104-119	537769737362 69748C6078X XXXXX0001h[14]	Namespace Globally Unique Identifier (NGUID)
120-127	8C6078XXXXXX 0001h[14]	IEEE Extended Unique Identifier (EUI64)
128-131	00090000h	LBA Format 0 Support (LBAF0)
132-191	All 00h	LBA Format 1 to 15 Support (LBAF1 - LBAF15)

[14] Values depend on device configuration.

Byte(s)	Default Value	Data Field Type Information
192–383	All 00h	Reserved
384–4095	All 00h	Vendor Specific (VS)

Table 18: Identify Controller Data Structure (CNS 01h)

Byte(s)	Default Value	Data Field Type Information
0–1	1DD4h	PCI Vendor ID (VID)
2–3	1DD4h	PCI Subsystem Vendor ID (SSVID)
4–23	XXXXh[14]	Serial Number (SN)
24–63	XXXXh[14]	Model Number (MN)
64–71	XXXXh[14]	Firmware Version (FR)
72	06h	Recommended Arbitration Burst (RAB)
73–75	8C6078h	IEEE OUI Identifier (IEEE)
76	00h	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	06h	Maximum Data Transfer Size (MDTS)
78–79	0000h	Controller ID (CNTLID)
80–83	00010400h	Version (VER)
84–87	000186A0h	Runtime D3 Resume Latency (RTD3R)
88–91	004C4B40h	Runtime D3 Entry Latency (RTD3E)
92–95	00000200h	Optional Asynchronous Events Supported (OAES)
96–99	00000002h	Controller Attributes (CTRATT)
100–101	0000h	Read Recovery Levels Supported (RRLS)
102–110	All 00h	Reserved
112–127	All 00h	FRU Globally Unique Identifier (FGUID)
128–129	0000h	Command Retry Delay Time 1 (CRDT1)
130–131	0000h	Command Retry Delay Time 2 (CRDT2)
132–133	0000h	Command Retry Delay Time 3 (CRDT3)
134–255	All 00h	Reserved
256–257	0017h	Optional Admin Command Support (OACS)
258	04h	Abort Command Limit (ACL)
259	07h	Asynchronous Event Request Limit (AERL)
260	14h	Firmware Updates (FRMW)
261	0Fh	Log Page Attributes (LPA)
262	FFh	Error Log Page Entries (ELPE)
263	04h	Number of Power States Supported (NPSS)
264	00h	Admin Vendor-Specific Command Configuration (AVSCC)
265	01h	Autonomous Power State Transition Attributes (APSTA)
266–267	016Bh	Warning Composite Temperature Threshold in Degrees Kelvin (WCTEMP)
268–269	017Fh	Critical Composite Temperature Threshold in Degrees Kelvin (CCTEMP)
270–271	0032h	Maximum Time for Firmware Activation (MTFA)
272–275	00000000h	Host Memory Buffer Preferred Size (HMPRE)
276–279	00000000h	Host Memory Buffer Minimum Size (HMMIN)
280–295	All 00h	Total NVM Capacity (TNVMCAP)
296–311	All 00h	Unallocated NVM Capacity (UNVMCAP)

Byte(s)	Default Value	Data Field Type Information
312–315	00000000h	Replay Protected Memory Block Support (RPMBS)
316–317	0005h	Extended Device Self-test Time (EDSTT)
318	01h	Device Self-test Options (DSTO)
319	00h	Firmware Update Granularity (FWUG)
320–321	0000h	Keep Alive Support (KAS)
322–323	0001h	Host Controlled Thermal Management Attributes (HCTMA)
324–325	012Fh	Minimum Thermal Management Temperature (MNTMT)
326–327	0175h	Maximum Thermal Management Temperature (MXTMT)
328–331	00000003h	Sanitize Capabilities (SANICAP)
332–335	000000000h	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)
336–337	0000h	Host Memory Maximum Descriptors Entries (HMMAXD)
338–339	0000h	NVM Set Identifier Maximum (NSETIDMAX)
340–341	0000h	Endurance Group Identifier Maximum (ENDGIDMAX)
342	00h	ANA Transition Time (ANATT)
343	00h	Asymmetric Namespace Access Capabilities (ANACAP)
344–347	00000000h	ANA Group Identifier Maximum (ANAGRPMAX)
348–351	00000000h	Number of ANA Group Identifiers (NANAGRPID)
352–355	00000000h	Persistent Event Log Size (PELS)
356–511	All 00h	Reserved
512	66h	Submission Queue Entry Size (SQES)
513	44h	Completion Queue Entry Size (CQES)
514–515	0000h	Maximum Outstanding Commands (MAXCMD)
516–519	000000001h	Number of Namespaces (NN)
520–521	005Fh	Optional NVM Command Support (ONCS)
522–523	0000h	Fused Operation Support (FUSES)
524	04h	Format NVM Attributes (FNA)
525	01h	Volatile Write Cache (VWC)
526–527	0001h	Atomic Write Unit Normal (AWUN)
528–529	0001h	Atomic Write Unit Power Fail (AWUPF)
530	00h	NVM Vendor-Specific Command Configuration (NVSCC)
531	00h	Namespace Write Protection Capabilities (NWPC)
532–533	0000h	Atomic Compare and Write Unit (ACWU)
534–535	0000h	Reserved
536–539	00000000h	Scatter Gather List Support (SGLS)
540–543	00000000h	Maximum Number of Allowed Namespaces (MNAN)
544–767	All 00h	Reserved
768–1023	XXXXh[14]	NVM Subsystem NVMe Qualified Name (SUBNQN)
1024–2047	All 00h	Reserved
2048–2079	XXXXh[14]	Power State 0 Descriptor
2080–2111	XXXXh[14]	Power State 1 Descriptor
2112–2143	XXXXh[14]	Power State 2 Descriptor
2144–2175	XXXXh[14]	Power State 3 Descriptor
2176–2207	XXXXh[14]	Power State 4 Descriptor

Byte(s)	Default Value	Data Field Type Information
2208-3071	All ooh	Power State 5 - 31 Descriptor (Not Applicable)
3072-4095	-	Vendor Specific (VS)

10. Health Monitoring Functionality

The N3002 M.2 SSDs support Self-Monitoring, Analysis, and Reporting Technology. The SSD supports log information as defined in the NVMe specification.

See the following table for the 512-byte data structure of the SMART/Health Information log page:

Table 19: SMART/Health Information (Log Identifier 02h)

Byte(s)	Description
0	Critical warning: for the state of the controller • Bit 0: If set to '1', then the available spare capacity has fallen below the threshold • Bit 1: If set to '1', then a temperature is greater than or equal to an over temperature threshold; or less than or equal to an under temperature threshold • Bit 2: If set to '1', then the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability. This bit can also be set on a failure of the energy management circuit. Please see chapter 10.1 Bit 3: If set to '1', then all of the media has been placed in read only mode
1-2	Composite Temperature: in degrees Kelvin
3	Available Spare: as a percentage of remaining spare capacity
4	Available Spare Threshold
5	Percentage Used: Estimate of the percentage of the NVM subsystem life left based on usage
6-31	Reserved
32-47	Data Units Read: Number of 512-byte sectors read by the host (in 1000 increments)
48-63	Data Units Written: Number of 512-byte sectors written by the host (in 1000 increments)
64-79	Host Read Commands: Number of Read commands completed by the controller
80-95	Host Write Commands: Number of Write commands completed by the controller
96-111	Controller Busy Time: Amount of time, in minutes, the controller was busy with I/O commands
112-127	Power Cycles: Number of power cycles that has occurred over the life of the drive
128-143	Power On Hours: Number of hours the device has been powered over the life of the drive (does not include the time the device is in low power state conditions)
144-159	Unsafe Shutdowns: Number of shutdowns that occurred without a shutdown notification
160-175	Media and Data Integrity Errors: Number of unrecoverable errors, including UECC, CRC checksum failures, and LBA mismatches, that occurred over the life of the drive
176-191	Number of Error Information Log Entries: Number of entries recorded in the Error Information log over the life of the drive
192-195	Warning Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Warning Composite Temperature Threshold (WCTEMP) but less than the Critical Composite Temperature Threshold (CCTEMP)
196-199	Critical Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Critical Composite Temperature Threshold (CCTEMP)
200-201	Temperature Sensor 1: Current controller Tjunction temperature, in degrees Kelvin
202-203	Temperature Sensor 2: Current composite temperature, in degrees Kelvin
204-205	Temperature Sensor 3: Current maximum NAND temperature, in degrees Kelvin
206-215	Not used

216-219	Thermal Management Temperature 1 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance
220-223	Thermal Management Temperature 2 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance
224-227	Total Time For Thermal Management Temperature 1: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance
228-231	Total Time For Thermal Management Temperature 2: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance
232-511	Reserved

The following data structure is applied to both Telemetry Host-Initiated log and Telemetry Controller-Initiated log:

Table 20: Telemetry Log (Log Identifier 07h)

Byte(s)	Description
Telemetry Header	
0	Log Identifier: This field shall be 07h
1-4	Reserved
5-7	IEEE OUI Identifier (IEEE):
4	Telemetry Host-Initiated Data Area 1 Last Block: This field shall be 0001h
10-381	Reserved
382	Telemetry Controller-Initiated Data Available
383	Telemetry Controller-Initiated Data Generation Number
384-511	Reserved
Telemetry Data Block 1	
528-529	Minimum Temperature, in degrees Kelvin
530-531	Current Temperature, in degrees Kelvin
532-533	Maximum Temperature, in degrees Kelvin
560-561	Number of valid spare blocks
562-563	Number of initial spare blocks
564-565	Run Time Bad Block Count
596-599	Maximum Erase Count on system blocks
604-607	Average Erase Count on system blocks
612-615	Maximum Erase Count on data storage blocks
620-623	Average Erase Count on data storage blocks
624-627	Rated Erase Count on system blocks
636-639	Rated Erase Count on data storage blocks
640	Remaining Life Percentage on system blocks based on P/E
641	Remaining Life Percentage based on spare blocks
646	Remaining Life Percentage on data storage blocks based on P/E
647	Cap Health Status (see PowerSafe Monitoring)

772-776	NVMe/PCIe Reset Count
804-807	PCIe Gen1 Link Speed Count
808-811	PCIe Gen2 Link Speed Count
812-815	PCIe Gen3 Link Speed Count
816-823	PCIe ECRC Event Count
824-831	PCIe LCRC Event Count
873	PCIe Power On Link Speed
876	PCIe Current Link Speed
877	PCIe Current Link Width
932-935	PCIe x1 Link Width Count
936-939	PCIe x2 Link Width Count
940-943	PCIe x4 Link Width Count
944-951	PCIe L1 Event Count

10.1 PowerSafe Monitoring

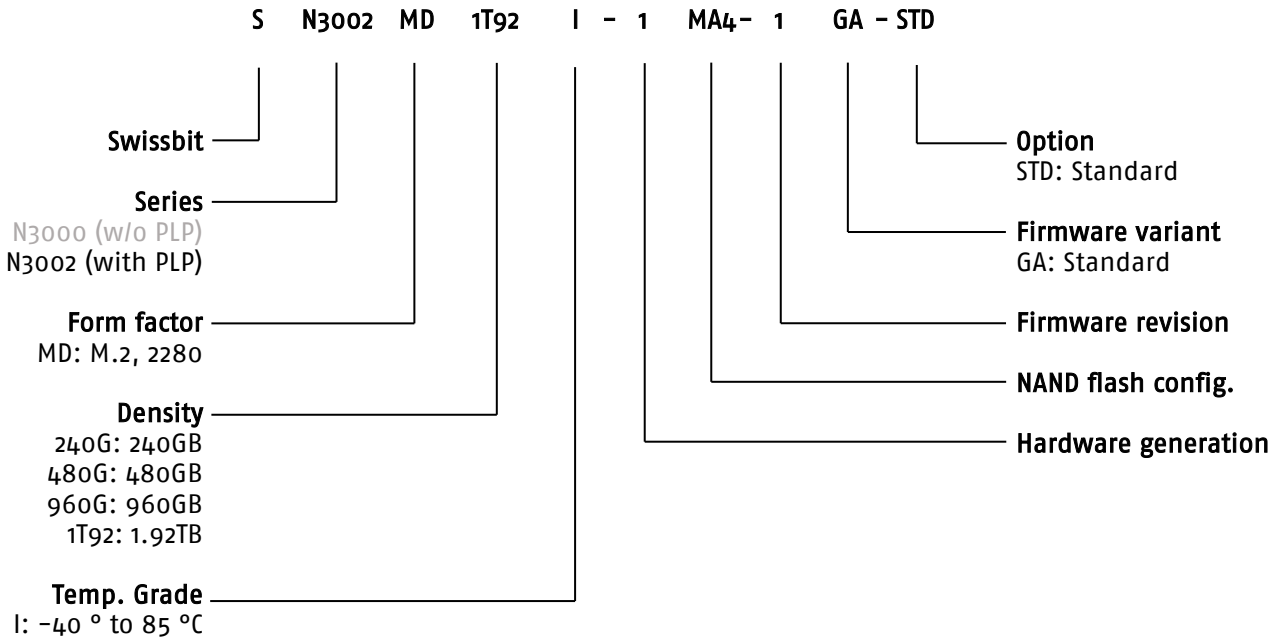
The Swissbit N-30m2 P powersafe™ series features an energy management circuit that allows the drive to flush all volatile data in case of a sudden power off event.

In case of an energy management circuit failure the drive will report a critical warning in the SMART/Health Information (Log Identifier 02h) log page. The "Critical Warning" field will report a value of 2h, "NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability".
In case of a critical warning please check the "Cap Health Status" field in Table 20: Telemetry Log (Log Identifier 07h):

- Cap Health Status bito = 1h: Capacitor health PASS
- Cap Health Status bito = oh: Capacitor health FAIL

First SMART/Health Information is reported after 30 seconds after power up.

11. Part Number Decoder



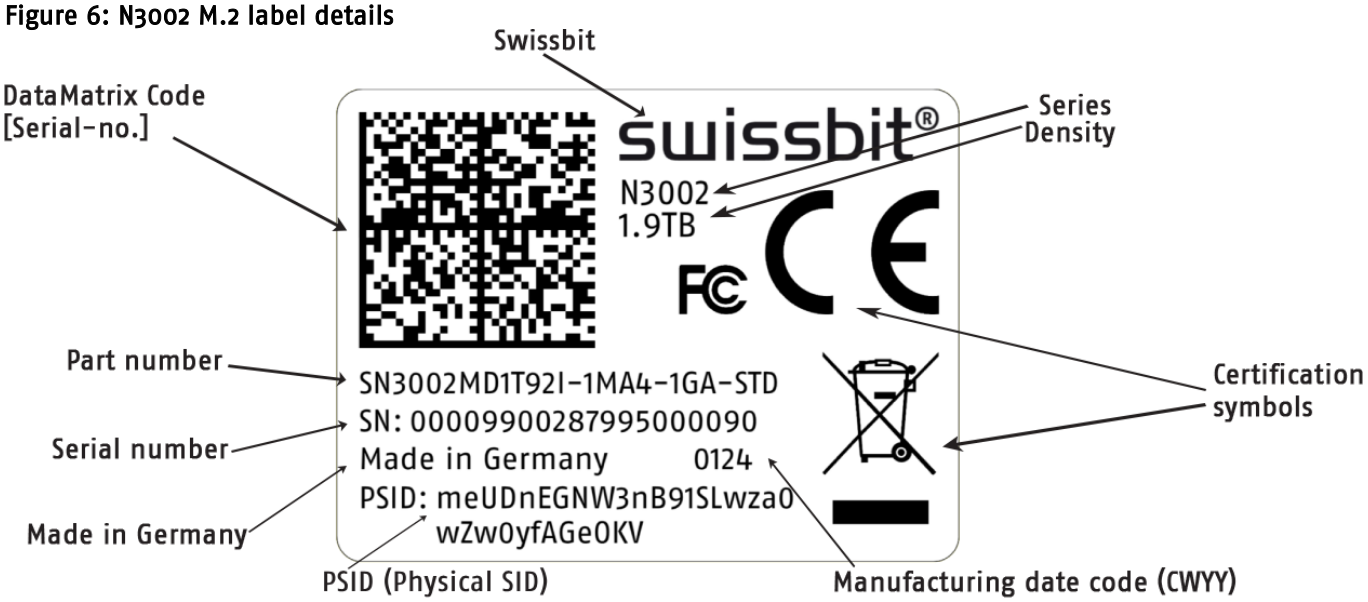
12. Marking Specification

12.1 Top View

Figure 5: N3002 M.2 top view

12.2 Print on the label

Figure 6: N3002 M.2 label details



13. Revision History

Table 21: Document Revision History

Date	Revision	Description	Revision Details
31-10-2023	0.90	Preliminary release	Doc. req. no. 6652
11-01-2024	0.91	PN Update	Doc. req. no. 6809
29-02-2024	0.92	SMART/Health Information has been updated	Doc. req. no. 6926
20-03-2024	0.93	Figure 1 Update	Doc. req. no. 6968
13-05-2024	1.00	Initial release	Doc. req. no. 7079