swissbit®

Product Fact Sheet

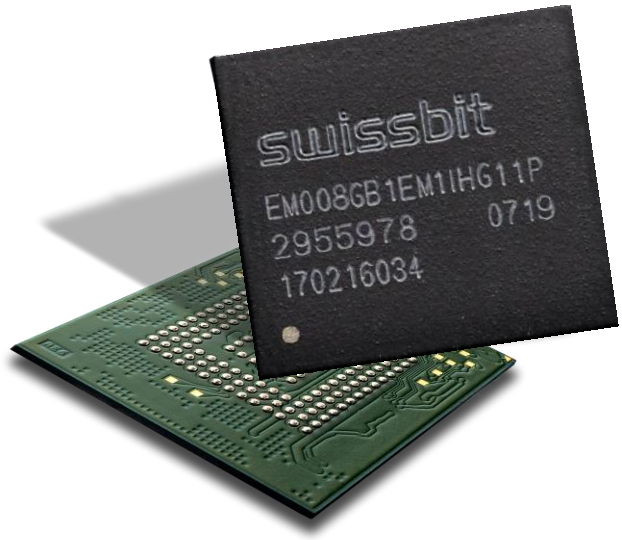
Industrial e•MMC Memory with Fast Boot

EM–10/16 Series

JEDEC e•MMC 4.41 compliant,
BGA 153 bal, 0.5mm pitch

Industrial Temperature Grade
(Autotmotive on request)

Date: October 11, 2019
Revision: 1.00



made in germany

Embedded MMC 4.41

EM-10/16 Industrial e·MMC Memory 4GB to 16GB (MLC), 2GB to 8GB (pSLC)

Main Features

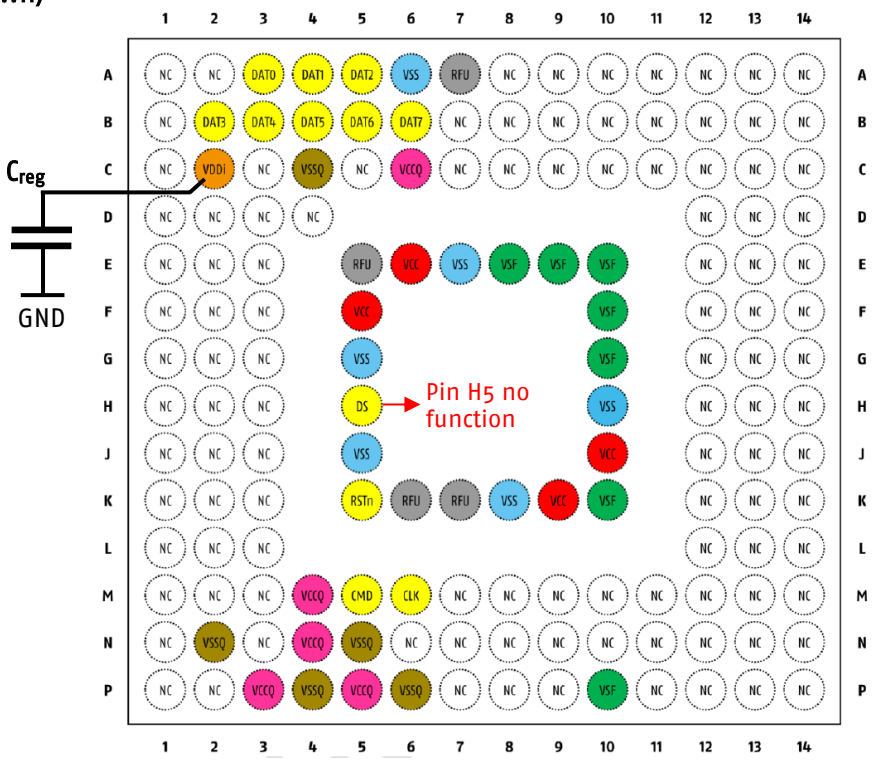
- Fully compliant with JEDEC **e·MMC 4.41** Standard (JESD84-A441)
- **153-ball BGA, 0.5mm pitch**
  11.5 x 13mm, RoHS compliant
- AEC-Q100 Grade 2 qualified
- Fast Boot feature for Instant-Up requirement
- Replaces common NOR Flash boot & NAND flash storage combination
- MLC and pSLC (Enhanced Mode) option to meet lifecycle and performance
- JEDEC e·MMC 4.41 specification, several features according JEDEC e·MMC 5.0
- Power Supply: (CMOS technology)
  - VCCQ 1.65V...1.95V or 2.7V...3.6V e·MMC supply
  - VCC 2.7V...3.6V NAND Flash supply

- **Optimized FW Algorithmic**
  - Fast Boot feature
    Proprietary controller function, which allows the host to start booting from the e·MMC in DDR mode within less than 10 ms after first command. Highly improved latency compared to standard e·MMC solutions. Targeting fast boot applications, e.g. fast loading of system-critical or safety-relevant data
  - Power loss protection incl. redundancy features and voltage detection to write protect the NAND flash
  - Firmware Protection Features (Redundant Anchor Block & Power-up check)
  - Diagnostic features with Life Time Monitoring tool support exceeding e·MMC standard
  - Advanced Wear Leveling technology
    Equal wear leveling of static and dynamic data.
    The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory, maximizing the write endurance of the device
  - Page Based Flash Management: by using page related flash management, write amplification for random write operations is minimized, allowing extended life time and high write performance
  - Read Disturb Management technology
    Read activity is monitored and the content is refreshed before critical disturbance levels occur
  - Dynamic Auto Refresh for data retention enhancement
    The interruptible background process maintains the user data for read disturb effects or retention degradation due to high temperature effects
  - Near Miss ECC technology
    Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes ECC margin levels and refresh data if necessary
  - Safe Shut-Down feature (on request)
    By issueing a special vendor command at immediate power-loss, a defined amount of data can be written to the device in a very short time. Can be used to save important system status data.

- **High reliability**
  - Designed for Industrial market and especially read intensive application like IIoT, gaming, medical and general boot medium use cases, NOR Flash replacement
  - Longevity, long life cycle, high data retention together with high temperature profile
  - Intensive write application should use the optional pSLC (Enhanced Mode) configuration
  - In-Field Firmware update without user data loss
  - Controlled BOM & PCN process
  - Industrial temperature from -40° up to 85°C (automotive grade up to 105°C on request)

- **Security Features (on request)**
  - Secure key storage: Digital signature, Encryption key, Authentication secrets, Unique ID
  - Secure functions: Sign(), Verifiy(), Encrypt(), Decrypt(), Authenticate()
  - Flash memory protection: Encryption, Access protection (read only, write only, write once, read/write)

Ballout (top view, ball down)



RFU pins: Reserved for Future Use, must be left floating on host (do not connect)
VSF pins: Vendor Specific Function, must generally be left floating on host (do not connect), further functionality options to be defined

System Performance

Max. System Performance	Instant-Up, MLC *	Sustained, MLC	Sustained, pSLC	Unit
Burst Data transfer Rate (max clock 52MHz)				MB/s
Sustained Sequential Read – operation DDR	90.5	n/a	n/a	
Sustained Sequential Write – operation DDR	n/a	n/a	n/a	
Sustained Sequential Read – operation SDR	n/a	49.4	49.4	
Sustained Sequential Write – operation SDR	n/a	14.3	31.1	
Random Read – operation DDR	n/a	n/a	n/a	IOPS 4k
Random Write – operation DDR	n/a	n/a	n/a	
Random Read – operation SDR	n/a	3096	3760	
Random Write – operation SDR	n/a	1105	1871	

*) The DDR interface with DDR-52 speed (104 MB/s) can be used for Fast Boot feature only (Read-only access)

Physical Dimensions

Physical Dimensions	Value	Unit
Length	13±0.1	mm
Width	11.5±0.1	
Thickness	Max. 1.3±0.15	

Recommended Temperature Conditions

Parameter	min	typ	max	Unit
Industrial Operating Temperature	-40	25	85*) (105)	°C
Storage Temperature	-40	25	85*) (105)	°C

*) high temperature storage without operation reduces the data retention, during operation the data will be refreshed if data degradation is detected.

e·MMC Features

e·MMC Feature	e·MMC 4.41	e·MMC 4.51	EM-10/16	e·MMC 5.0	e·MMC 5.1
Bus Width	x1/x4/x8				
Clock Frequency	~52MHz	~200MHz	~52MHz	~200MHz	~200MHz
Max bandwith	104 MB/s	200 MB/s	52 MB/s *	400 MB/s	400 MB/s
H/W reset	Yes				
DDR Interface	Optional	Optional	No *	Optional	Optional
High Speed Mode (HS200)	-	Optional	-	Optional	Optional
High Speed Mode (HS400), DS Pin	-	-	-	Optional	Optional
Command Queuing	-	-	-	-	Optional
Sleep Mode	Yes				
Reliable Write	Yes				
Write Protect	Yes				
Multiple Partitions (GP und Boot, RPMB)	Optional	Yes	Yes	Yes	Yes
Enhanced Mode / Storage Option pSLC Config Option	Optional	Yes	On request	Yes	Yes
Secure Erase / Secure TRIM	Optional	Optional	Yes	Optional	Optional
Replay Protect Memory Block	Yes				
Alternate Boot Operation	Yes				
Background Operations	Optional	Yes	Yes	Yes	Yes
High Priority Interrupt	Optional	Yes	Yes	Yes	Yes
Discard	-	Yes	Yes	Yes	Yes
Sanitize	-	Optional	Yes	Optional	Optional
Power Off Notification	-	Yes	Yes	Yes	Yes
Production State Awareness	-	-	Yes	Optional	Optional
Field Firmware Update (by eMMC protocol)	-	-	Proprietary, eMMC compliant on request	Optional	Optional
Device Health Report	-	-	Yes (extended)	Optional	Optional
Secure Removal Type	-	-	On request	Optional	Optional

*) The DDR interface with DDR-52 speed (104 MB/s) can be used for Fast Boot feature only (Read-only access)

For more information on e·MMC interface, please visit JEDEC homepage (www.jedec.org)

Why Swissbit?

Swissbit strives to create innovative technologies for future market opportunities utilizing a highly skilled in-house product research and development team. Swissbit maintains a marketing edge by continuing to manufacture world-class high quality memory products and providing customers with both high value and low cost of ownership achieved through efficient processes and procedures.